

Application Number
09/416,368

Applicant **Corisis et al.**

Filing Date **October 12, 1999**

Group Art Unit 2812

U.S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO

OTHER DOCUMENTS

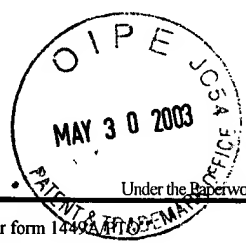
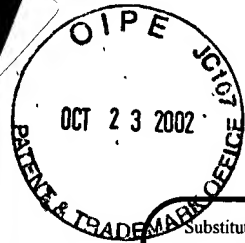
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 5

Complete if Known

Application Number	09/416,368
Filing Date	October 12, 1999
First Named Inventor	David J. Corisis et al.
Group Art Unit	2827
Examiner Name	D. Graybill
Attorney Docket Number	3770.2US (97-0332.2)

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
C		US- 3,932,934	01/20/1976	Lynch et al.	
		US- 4,142,286	03/06/1979	Knuth et al.	
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		US- 4,722,135	02/02/1988	Read	
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FOREIGN PATENT DOCUMENTS

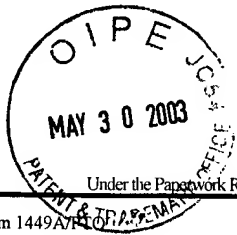
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		Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)				

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		Number - Kind Code ² (if known)			
[Handwritten mark]		US- 5,255,431	10/26/1993	Burdick	
		US- 5,329,423	07/12/1994	Scholz	
		US- 5,337,219	08/09/1994	Carr et al.	
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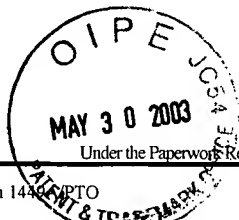
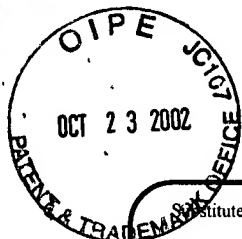
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Sheet 3 of 5

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Group Art Unit	2827
Examiner Name	D. Graybill
Attorney Docket Number	3770.2US (97-0332.2)

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	4	US- 5,637,008	06/10/1997	Kozel	
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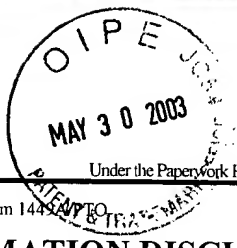
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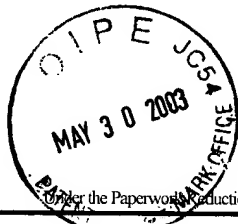
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Sheet 5 of 5

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Examiner Name	D. Graybill
Attorney Docket Number	3770 21US (97-0332 2)

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
G		PUTTLITZ et al., "C-4/CBGA Comparison with Other MLC Single Chip Package Alternatives," <u>IEEE Transactions on Components, Packaging, and Manufacturing Technology</u> , May 1995, pps. 250-256, Part B, Vol. 18, No.2.	
G		GOLDMANN, Lewis S., "Statistical Model for the Inherent Tilt of Flip-Chips," <u>Transactions of the ASME Journal of Electronic Packaging</u> , March 1996, pps. 16-20, Vol. 118.	
G		NASIATKA et al., "Determination of Optimal Solder Volume for Precision Self-Alignment of BGA using Flip-Chip Bonding," pps. 6-9.	

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